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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,052	12/28/2000	Ravi Kumar Arimilli	AUS920000679US1	9307

42640 7590 04/27/2005

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,052	ARIMILLI ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Notice of Appeal as received on 11/19/2004 and Appeal Brief as received on 2/24/2005.

Response to Arguments

3. In view of the appeal brief filed on February 24, 2005, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. The examiner asserts that errors may exist within the specification. For instance, on page 15, line 1, should "compete" be replaced with --complete--?

Claim Objections

5. Claim 1 is objected to because of the following informalities: In line 2, replace "a first operational characteristics" with --first operational characteristics--. Also, in the second to last line, replace "provides" with --provide--. Appropriate correction is required.

6. Claim 2 is objected to because it is unclear as to whether applicant is trying to introduce another "second, heterogenous processor" (in lines 1-2), or whether applicant is referring to the same second, heterogenous processor of claim 1. If the latter, then applicant should use "the" or "said" language, in claim 2, as opposed to "a" language.

7. Claim 3 is objected to because of the following informalities: In line 4, replace "begin" with --being--. In the last line, the word "having" seems to be grammatically inappropriate. Appropriate correction is required.

8. Claim 5 is objected to because of the following informalities: In line 4, replace "comprising system data bus" with --comprising a system data bus--. Appropriate correction is required.

9. Claim 6 is objected to because of the following informalities: In line 2, replace "indicating" with --indicate--. Also, in line 4, applicant should replace "cache line" with either --cache lines-- or --a cache line--. Appropriate correction is required.

10. Claim 7 is objected to because of the following informalities: In line 1, replace "includes" with --include--. In line 6, replace "utilizes" with --utilize--. Appropriate correction is required.

11. Claim 10 is objected to because of the following informalities: In line 17, replace "provides" with --provide--. Appropriate correction is required.

12. Claim 11 is objected to because of the following informalities: In line 3, replace "comprising system data bus" with --comprising a system data bus--. In line 9, replace "indicating" with --indicate--. Also, in the last line, the examiner believes the word "to" should be removed. Appropriate correction is required.

13. Claim 12 is objected to because of the following informalities: In line 8, replace "that designed" with --that are designed--. In line 9, replace "advance operation" with --advanced operational--. Also, in lines 8-9, when applicant mentions "said plurality of processors", is applicant referring to the heterogenous processors. If so, applicant should insert "heterogenous" for increased clarity, as lines 8-9 are very confusing to the examiner. Finally, in the second to last line of claim 12, replace "provides" with --provide--. Appropriate correction is required.

14. Claim 13 is objected to because of the following informalities: The examiner believes that applicant is referring to the plurality of heterogenous processors when claiming "said plurality of processors". If so, it is asked that applicant add the word "heterogenous" in claim 13 for increased clarity. Appropriate correction is required.

15. Claim 14 is objected to because of the following informalities: The examiner believes that applicant is referring to the plurality of heterogenous processors when claiming "said plurality of processors". If so, it is asked that applicant add the word "heterogenous" in claim 14 for increased clarity. Appropriate correction is required.

16. Claim 15 is objected to because of the following informalities: In the last line, replace "processors" with --processor's--. In the last line, the word "having" seems to be grammatically inappropriate. Appropriate correction is required.

17. Claim 17 is objected to because of the following informalities: In line 3, replace "comprising system data bus" with --comprising a system data bus--. Appropriate correction is required.

18. Claim 19 is objected to because of the following informalities: In line 2, replace "indicating" with --indicate--. Also, in line 4, applicant should replace "cache line" with either --cache lines-- or --a cache line--. Appropriate correction is required.

19. Claim 20 is objected to because of the following informalities: In line 1, replace "includes" with --include--. In line 5, replace "utilizes" with --utilize--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

20. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

21. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

22. Claims 1, 10, and 12 refer to forward compatibility amongst said first processor and the second, heterogenous processor. Nowhere in applicant's original specification was there support for forward compatibility amongst heterogenous processors.

23. Claims 4 and 15 refer to each bus including one or more pins that are set/reset to indicate a particular condition of a connected component. The examiner has been unable to find support for such a feature. The examiner was able to find a master processor select bus/pin 616C which indicates which processor is the master. However, there is no mention of the other pins being set/reset to indicate conditions. If the examiner has overlooked the portion of the specification which supports this feature, it is asked that applicant bring it to the examiner's attention.

24. Claims 7 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, each of claims 7 and 20 refer to robust out-of-order processing. The examiner has been unable to determine what this type of processing constitutes, as applicant's specification only includes the following sentence: " Also heterogeneity supports processors operating with in-order execution, some out-of-order execution, or robust out-of-order execution." There is no definition of robust

out-of-order processing and since the examiner is unclear as to what it means, the specification is non-enabling.

25. All remaining claims are rejected under 112, first paragraph for being dependent on claims which are rejected under 112, first paragraph.

26. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

27. Claims 3-8 and 10-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

28. Claim 3 recites the limitation "said second cache" in line 8. There is insufficient antecedent basis for this limitation in the claim because applicant uses the language "including one or more of", and when certain ones are picked, this problem occurs. For instance, if the claimed configuration only included "said second cache supporting cache intervention...", then there is no antecedent basis for "said second cache".

29. Claim 4 is rejected under 112, 2nd paragraph, for dependent upon a claim which is rejected under 112, 2nd paragraph.

30. Claim 5 recites the limitation "said pins" in line 2. There is insufficient antecedent basis for this limitation in the claim because applicant previously claims "a first set of pins" (claim 5) and "one or more pins" (claim 4). Consequently, if applicant is referring to the first set of pins, then "one of said pins" should be changed to --one of said first set of pins--. However, if

applicant is referring to the one or more pins, then "one of said pins" should be changed to --one of said one or more pins--.

31. Claim 6 is rejected under 112, 2nd paragraph, for dependent upon a claim which is rejected under 112, 2nd paragraph.

32. Claim 7 recites the limitation "said operational characteristics" in line 1. There is insufficient antecedent basis for this limitation in the claim because it is not clear whether this refers to "first operational characteristics" in claim 1 (corresponding to the first processor) or the "operational characteristics" of claim 2 (for the second processor).

33. Claim 8 is rejected under 112, 2nd paragraph, for dependent upon a claim which is rejected under 112, 2nd paragraph.

34. Claim 10 recites the limitation "said interrupt pins" in lines 4-5, the limitation "said new, heterogenous processor" in lines 7-8, the limitation "said first processor" in lines 11 and 16, the limitation "said second processor" in line 11, the limitation "the SMP" in line 12, the limitation "the interconnection means" in line 13, and the limitation "said second, heterogenous processor" in line 16. There is insufficient antecedent basis for these limitations in the claim.

35. Claim 11 recites the limitation "The method of claim 7" in line 1. There is insufficient antecedent basis for this limitation in the claim because there is no method in claim 7. Please change "The method of Claim 7" to --The method of Claim 10--. Claim 11 also recites the limitation "said pins" in line 7. There is insufficient antecedent basis for this limitation in the claim because applicant previously claims "a first set of pins" (line 6) and "one or more pins" (line 4). Consequently, if applicant is referring to the first set of pins, then "one of said pins"

should be changed to --one of said first set of pins--. However, if applicant is referring to the one or more pins, then "one of said pins" should be changed to --one of said one or more pins--.

36. Claim 12 recites the limitation "said first processor" in lines 11 and 16, the limitation "said second processor" in line 11, the limitation "the SMP" in line 12, and the limitation "the interconnection means" in line 13. There is insufficient antecedent basis for these limitations in the claim.

37. Claim 13 is rejected under 112, 2nd paragraph, for dependent upon a claim which is rejected under 112, 2nd paragraph.

38. Claim 14 is rejected under 112, 2nd paragraph, for dependent upon a claim which is rejected under 112, 2nd paragraph.

39. Claim 15 recites the limitation "the first processor" in lines 4 and 10-11, and the limitation "the second processor" in lines 5-6 and 11. There is insufficient antecedent basis for these limitations in the claim. In addition, claim 15 recites the limitation "said second cache" in line 8. There is insufficient antecedent basis for this limitation in the claim because applicant uses the language "including one or more of", and when certain ones are picked, this problem occurs. For instance, if the claimed configurations only included "said second cache supporting cache intervention...", then there is no antecedent basis for "said second cache".

40. Claim 16 is rejected under 112, 2nd paragraph, for dependent upon a claim which is rejected under 112, 2nd paragraph.

41. Claim 17 recites the limitation "said interconnect means" in line 1. There is insufficient antecedent basis for this limitation in the claim.

42. Claim 18 recites the limitation "said pins" in line 2. There is insufficient antecedent basis for this limitation in the claim because applicant previously claims "a first set of pins" (claim 18) and "one or more pins" (claim 17). Consequently, if applicant is referring to the first set of pins, then "one of said pins" should be changed to --one of said first set of pins--. However, if applicant is referring to the one or more pins, then "one of said pins" should be changed to --one of said one or more pins--.

43. Claim 19 recites the limitation "the respective pin" in line 2. There is insufficient antecedent basis for this limitation in the claim.

44. Claim 20 recites the limitation "said operational characteristics" in line 1. There is insufficient antecedent basis for this limitation in the claim as it is not clear whether applicant is referring to the different operational characteristics of claim 1 or the advanced operational characteristics of claim 1. Claim 20 also recites the/said first processor and the/said second processor throughout the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

45. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

46. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory, U.S. Patent No. 6,513,057 (as applied in the previous Office Action and herein

referred to as McCrory) in view of Derrick et al., U.S. Patent No. 5,704,058 (as applied in the previous Office Action and herein referred to as Derrick), and further in view of Cochcroft, Jr. et al., U.S. Patent No. 5,317,738 (herein referred to as Cochcroft).

47. Referring to claim 12, McCrory has taught has taught a multiprocessor system comprising:

a) a plurality of heterogenous processors with different operational characteristics and physical topology connected on a system planar. See the abstract, Fig.3, and column 5, line 66, to column 6, line 8.

b) a system bus that supports system centric operations. See Fig.3 and column 2, lines 36-67.

c) interrupt pins coupled to said system bus that provide connection for at least one of said plurality of heterogenous processors. See column 2, lines 40-47, and note that processors are coupled through an interface (interrupt pins) to the rest of the system.

d) an enhanced system bus protocol that supports downward compatibility of newer processors that support advanced operational characteristics from among said plurality of processors to processors that do not support said advance operation characteristics. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are backward compatible with 80486. In addition, the system clearly supports forward compatibility because the system can still employ SMP even though a newer family (Pentium) is used with an older family (80486).

e) McCrory has not taught an enhanced operating system (OS) that supports inter-processing operations between said first processor and said second processor including cache coherency operations based on a collective memory configuration of the SMP. However, Derrick has

taught the concept of employing cache coherency in a multiprocessor system. See column 1, lines 15-27. Cache coherency is employed so that all caches contain consistent, up-to-date data. Otherwise, if a particular cache did not have the most up-to-date data, the processor accessing that cache would be performing operations using incorrect data, which would cause delays in execution. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS to include support for cache coherency.

f) McCrory has not taught that said OS logs operating characteristics and cache topology data of each processor connected to the interconnection means to calculate a most efficient work allocation among processors. However Cochcroft has taught a system in which process identification codes (operating characteristics) are logged and the number of cache lines used by each process in each processor (cache topology data) is logged. This data allows for efficient allocation of workload to the processors. See column 1, lines 6-9. As a result, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS log the aforementioned data.

g) McCrory has further taught that said enhanced system bus protocol and said enhanced operating system support backward and forward compatibility amongst a first processor and a second, heterogenous processor. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are backward compatible with 80486. In addition, the system clearly supports forward compatibility because the system can still employ SMP even though a newer family (Pentium) is used with an older family (80486).

h) McCrory has not taught providing system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states. However, Official Notice

is taken that prefetching is well known and accepted in the art. Prefetching allows for fetching of instructions/data before the instructions/data are actually needed. Therefore, at the time when they are needed, they are already fetched and present in the system, thereby avoiding any waiting time that might be incurred due to fetching instructions/data as they are needed. In addition, Derrick has taught cache intervention in a multiprocessor system. See column 5, lines 4-14, and note that any L2 cache may intervene and provide the requested data. As is known, cache intervention allows an updated cache to provide data to a requesting device whose cache is not updated. This also prevents the requesting device from having to spend many cycles accessing main memory for the data. Finally, Derrick has taught an intelligent cache state enhancement. See the abstract and column 3, lines 7-17 and note the implementation of an arbitration scheme for snoop activity. Such a scheme allows for optimized performance and efficient allocation of bandwidth. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory to include cache intervention and a cache arbitration scheme which optimize system performance.

48. Referring to claim 14, McCrory in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 12. Although McCrory in view of Derrick and further in view of Cochcroft has taught that said plurality of processors includes different numbers of processors on a single processor chip (see Fig.4), they have not explicitly taught that said plurality of processors includes heterogenous processor topologies including different cache sizes, cache states, and number of cache levels. However, McCrory has taught using heterogenous processors from different families together in a SMP system. See column 2, lines 27-47, and the abstract. And, Official Notice is taken that different processors exhibit different

characteristics such as the ones listed above. Since, certain families of processors would be picked by the designer for executing different types of applications, the characteristics that ultimately exist are based on designer choice. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to include heterogeneous processors that include different cache sizes, cache states, and cache levels among the different processors because processors differ in these areas, and different processors may be selected by the designer.

49. Claims 1-7, 9-11, 13, 15, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory, in view of Derrick in view of Cochcroft, as applied above, and further in view of Bacot et al., U.S. Patent No. 5,235,687 (herein referred to as Bacot).

50. Referring to claim 1, McCrory has taught a data processing system comprising:

a) a first processor with a first operational characteristics on a system planar. See Fig.3, the abstract, column 2, lines 37-47, and column 5, line 66, to column 6, line 8.

b) interconnection means for connecting a second, heterogenous processor on said system planar, wherein said interconnection means enables said first processor and said second, heterogenous processor to collectively operate as a symmetric multiprocessor (SMP) system. See Fig.3, the abstract, column 2, lines 37-47, and column 5, line 66, to column 6, line 8. McCrory has not explicitly taught later connecting a second, heterogenous processor on said system planar, wherein said interconnection means enables said first processor and said second, heterogenous processor to collectively operate as a symmetric multiprocessor (SMP) system. However, Bacot has taught a multiprocessor system in which, when an individual processor breaks or becomes

defective, that individual processor is replaced so that the system can return to operating at full capacity. See column 1, lines 57-68. A person of ordinary skill in the art would have recognized that if a processor breaks in McCrory, then the broken processor could be replaced with a functioning processor, thereby allowing symmetric multiprocessing. As a result, in case of individual processor breakage, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory such that a second, heterogenous processor is later added in to the system via interconnection means to allow the system to perform at a higher level.

c) McCrory has not taught an enhanced operating system (OS) that supports inter-processing operations between said first processor and said second processor including cache coherency operations based on a collective memory configuration of the SMP. However, Derrick has taught the concept of employing cache coherency in a multiprocessor system. See column 1, lines 15-27. Cache coherency is employed so that all caches are contain consistent up-to-date data. Otherwise, if a particular cache did not have the most up-to-date data, the processor accessing that cache would be performing operations using incorrect data, which would cause delays in execution. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS to include support for cache coherency.

d) McCrory has not taught that said OS logs operating characteristics and cache topology data of each processor connected to the interconnection means to calculate a most efficient work allocation among processors. However Cochcroft has taught a system in which process identification codes (operating characteristics) are logged and the number of cache lines used by each process in each processor (cache topology data) is logged. This data allows for efficient

allocation of workload to the processors. See column 1, lines 6-9. As a result, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS log the aforementioned data.

e) McCrory has further taught said interconnection means and said enhanced operating system support backward and forward compatibility amongst said first processor and said second, heterogenous processor. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are backward compatible with 80486. In addition, the system clearly supports forward compatibility because the system can still employ SMP even though a newer family (Pentium) is used with an older family (80486).

f) McCrory has not taught providing system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states. However, Official Notice is taken that prefetching is well known and accepted in the art. Prefetching allows for fetching of instructions/data before the instructions/data are actually needed. Therefore, at the time when they are needed, they are already fetched and present in the system, thereby avoiding any waiting time that might be incurred due to fetching instructions/data as they are needed. In addition, Derrick has taught cache intervention in a multiprocessor system. See column 5, lines 4-14, and note that any L2 cache may intervene and provide the requested data. As is known, cache intervention allows an updated cache to provide data to a requesting device whose cache is not updated. This also prevents the requesting device from having to spend many cycles accessing main memory for the data. Finally, Derrick has taught an intelligent cache state enhancement. See the abstract and column 3, lines 7-17 and note the implementation of an arbitration scheme for snoop activity. Such a scheme allows for optimized performance and efficient allocation of

bandwidth. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory to include cache intervention and a cache arbitration scheme which optimize system performance.

51. Referring to claim 2, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory has further taught a second, heterogenous processor connected to said system bus via said interconnect means, wherein said second, heterogenous processor is comprises more advanced physical and operational characteristics than said first processor, wherein said different physical component parameters include one or more of a higher number of cache levels, larger cache sizes, improved cache hierarchy, cache intervention, and larger number of on-chip processors. See Fig.4 and column 6, lines 28-33, and note that the second processor may be a Pentium-type processor, whereas the first processor may be an 80486-type processor (each processor has different operational characteristics). In addition, looking at Fig.4, the second processor 312 has a larger number of on-chip processors than the first processor 314.

52. Referring to claim 3, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory and Derrick have further taught a cache coherency protocol that supports non-homogenous cache configuration amongst heterogenous processors, said non-homogenous cache configurations including different levels of caches (Derrick, Fig.1), cache states (coherent and incoherent, for instance), and shared caches among processors. See Derrick, column 1, lines 15-57, and column 3, lines 7-17.

53. Referring to claim 4, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 3. McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has further taught that said interconnect means is coupled to a system bus and comprises a plurality of buses for connecting additional processors to said system bus, said buses comprising a system data bus and base address bus (McCrory, column 6, lines 12-16), a base snoop response bus and extended snoop response bus (Derrick, column 4, lines 45-46, and column 5, lines 16-18). McCrory has further taught a mater processor select bus (column 8, lines 30-50). Note that an interrupt signal (inherently received on a bus) is used to switch processors (to a "master processor") if the current processor cannot execute subsequent code (non-native code). In addition, there would be a bus which is used to send a signal to the processor which is being switched to.

54. Referring to claim 5, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 4. McCrory has further taught that said master processor select bus includes a first set of pins, each connected to an added processor, wherein when one of said pins is set to an active state, the connected processor operates as a master on the master processor select bus. See column 8, lines 30-50, and note that any of the processors in the system may be switched to in order to execute code native to that processor. Consequently, each processor would be connected to a pin/bus that when active, tells that processor that it will be executing the native code.

55. Referring to claim 6, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 5. Derrick has further taught that:

a) a respective pin is set when a read operation is issued to indicate that the issuing processor is the master processor. See column 5, lines 4-10, and note that a GNT pin is set after a requesting device makes its request (read operation) and the requesting device is granted control.

b) when said read operation is snooped by a second added processor with a cache line in R coherency state, the second added processor drives the extended snoop response bus with shared intervention information and sends a retry response on the base snoop response bus. See column 5, lines 14-18, and note that when another cache has the data requested by the requesting device (in the "R coherency state"), the data is driven onto the extended snoop response bus 126 (Fig.1) and a response ("retry response") is driven on the base snoop response bus HITM# (Fig.2).

56. Referring to claim 7, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 6. McCrory has further taught that said operational characteristics include operating frequency, wherein the second processor operates at a higher frequency that said first processor. See column 5, line 66, to column 6, line 8, and note the different operating frequencies.

57. Referring to claim 9, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory and Bacot has further taught a switch that provides direct point-to-point connection between said first processor and later added processors. See Fig.3, column 2, lines 40-47, and column 6, lines 12-20, and note that processors are added to the system via connector (switch) which allows for point-to-point communication. For instance, in column 6, lines 12-15, McCrory states that processors communicate with one another. One could call the first processor point A and a later added

processor point B. Point A would then communicate with point B (point-to-point communication) via the hardware that connects the points. The bus and connectors (switches).

58. Referring to claim 10, McCrory has taught a method for upgrading processing capabilities of a data processing system comprising:

a) providing a plurality of pins from a system bus on a system planar to allow addition of processors. See the abstract and Fig.3 and note that processors may be added to the system via bus/pins. McCrory has not taught allowing for later addition of other processors. However, Bacot has taught a multiprocessor system in which, when an individual processor breaks or becomes defective, that individual processor is replaced so that the system can return to operating at full capacity. See column 1, lines 57-68. A person of ordinary skill in the art would have recognized that if a processor breaks in McCrory, then the broken processor could be replaced with a functioning processor, thereby allowing symmetric multiprocessing. As a result, in case of individual processor breakage, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory such that a second, heterogenous processor is later added in to the system via interconnection means to allow the system to perform at a higher level.

b) enabling direct connection of a new, heterogenous processor to said system planar via said interrupt pins, wherein said interrupt pins provide communication paths between said heterogenous processor and other processors previously attached to said system planar. See McCrory, column 2, lines 27-47, the abstract, and column 6, lines 12-20.

c) providing support for full backward compatibility by said heterogenous processor when said processor comprises more advanced operational characteristics to enable said data processing

system to operate as a symmetric multiprocessor system. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are more advanced yet backward compatible with 80486. In addition, the system clearly supports forward compatibility because the system can still employ SMP even though a newer family (Pentium) is used with an older family (80486). In addition, from the abstract, note that the heterogenous processors allow for symmetric multiprocessing.

d) McCrory has not taught support includes an enhanced operating system (OS) that supports inter-processing operations between said first processor and said second processor including cache coherency operations based on a collective memory configuration of the SMP. However, Derrick has taught the concept of employing cache coherency in a multiprocessor system. See column 1, lines 15-27. Cache coherency is employed so that all caches are contain consistent up-to-date data. Otherwise, if a particular cache did not have the most up-to-date data, the processor accessing that cache would be performing operations using incorrect data, which would cause delays in execution. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS to include support for cache coherency.

e) McCrory has not taught that said OS logs operating characteristics and cache topology data of each processor connected to the interconnection means to calculate a most efficient work allocation among processors. However Cochcroft has taught a system in which process identification codes (operating characteristics) are logged and the number of cache lines used by each process in each processor (cache topology data) is logged. This data allows for efficient allocation of workload to the processors. See column 1, lines 6-9. As a result, in order to

increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS log the aforementioned data.

f) McCrory has further taught said interconnection means and said enhanced operating system support backward and forward compatibility amongst said first processor and said second, heterogenous processor. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are backward compatible with 80486. In addition, the system clearly supports forward compatibility because the system can still employ SMP even though a newer family (Pentium) is used with an older family (80486).

g) McCrory has not taught providing system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states. However, Official Notice is taken that prefetching is well known and accepted in the art. Prefetching allows for fetching of instructions/data before the instructions/data are actually needed. Therefore, at the time when they are needed, they are already fetched and present in the system, thereby avoiding any waiting time that might be incurred due to fetching instructions/data as they are needed. In addition, Derrick has taught cache intervention in a multiprocessor system. See column 5, lines 4-14, and note that any L2 cache may intervene and provide the requested data. As is known, cache intervention allows an updated cache to provide data to a requesting device whose cache is not updated. This also prevents the requesting device from having to spend many cycles accessing main memory for the data. Finally, Derrick has taught an intelligent cache state enhancement. See the abstract and column 3, lines 7-17 and note the implementation of an arbitration scheme for snoop activity. Such a scheme allows for optimized performance and efficient allocation of bandwidth. As a result, it would have been obvious to one of ordinary skill in the art at the time

of the invention to modify McCrory to include cache intervention and a cache arbitration scheme which optimize system performance.

59. Referring to claim 11, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a method as described in claim 10. Furthermore, claim 11 recites limitations previously recited in claims 4, 5, and 6. Consequently, claim 11 is rejected for the same reasons set forth in the rejections of claims 4, 5, and 6 above.

60. Referring to claim 13, McCrory in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory has further taught a switch that provides direct point-to-point connection between each of said plurality of processors. See Fig.3, column 2, lines 40-47, and column 6, lines 12-20, and note that processors are added to the system via connector (switch) which allows for point-to-point communication. For instance, in column 6, lines 12-15, McCrory states that processors communicate with one another. One could call the first processor point A and a later added processor point B. Point A would then communicate with point B (point-to-point communication) via the hardware that connects the points. The bus and connectors (switches). McCrory has not taught connection between each of said plurality of processors and later added processors. However, Bacot has taught a multiprocessor system in which, when an individual processor breaks or becomes defective, that individual processor is replaced so that the system can return to operating at full capacity. See column 1, lines 57-68. A person of ordinary skill in the art would have recognized that if a processor breaks in McCrory, then the broken processor could be replaced with a functioning processor, thereby allowing symmetric multiprocessing. As a result, in case of individual processor breakage, it would have been obvious to one of ordinary skill in the art at the time of

the invention to modify McCrory such that a second, heterogenous processor is later added in to the system via interconnection means to allow the system to perform at a higher level.

61. Referring to claim 15, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 13. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 3 above.

62. Referring to claim 17, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 15. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 4 above.

63. Referring to claim 18, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 17. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 5 above.

64. Referring to claim 19, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 18. Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 6 above.

65. Referring to claim 20, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 19. Furthermore, claim 20 is rejected for the same reasons set forth in the rejection of claim 7 above.

66. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory in view of Bacot in view of Derrick and further in view of Cochcroft, as applied above, and further in view of MacWilliams et al., U.S. Patent No. 5,228,134 (herein referred to as MacWilliams).

67. Referring to claim 8, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 3. The aforementioned have not taught that all caches are sectored into widths representing a smallest width cache line that is accessible within the overall system. However, caches are inherently divided into lines having widths, and MacWilliams has taught that conventional parallel cache implementations (plurality of caches) force the line size to be the same. A person of ordinary skill in the art would have recognized that this would allow for a less complex accessing scheme. That is, if all caches are the same size, then accessing is made simple. However, if line sizes were different in each cache, then a more complex scheme would need to be employed. As a result, because MacWilliams has taught that convention systems force cache lines of caches to be the same size, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory to include such a feature.

68. Referring to claim 16, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 15. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 8 above.

Conclusion

69. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Stiffler et al., U.S. Patent No. 4,484,273, has taught a multi-processor computer system is disclosed in which processing elements, memory elements and peripheral units can be physically added and removed from the system without disrupting its operation or necessitating any reprogramming of software running on the system, wherein the processing elements simultaneously perform data processing calculations for a plurality of data processing tasks.

Gorishek, IV et al., U.S. Patent No. 6,308,255, has taught a symmetrical multiprocessing bus and chipset used for coprocessor support allowing non-native code to run in a system. Both homogenous and heterogenous processors may be later added wherein a SMP system may be realized.

Huang et al., U.S. Patent No. 5,761,479, has taught upgradeable/downgradeable central processing unit chip computer systems.

Mori et al., U.S. Patent No. 4,716,526, has taught a multiprocessor system in which different types of processors may be later added to the system and used in a switching type execution environment.

Intel, "Multiprocessor Specification," Version 1.4, May 1997, has disclosed supporting unequal processors in an SMP system.

Intel, "Intel® Pentium® II Xeon™ Processor Integration Notes," January 1999, has taught mixing processors of multiple cache size and also processors with different steppings.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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